REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV																						
PAGE																						
REV STATUS OF PAGES	**REV**																					
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14							

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 10-12-07	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, VARIABLE RESOLUTION, 10-BIT TO 16-BIT R/D CONVERTER WITH REFERENCE OSCILLATOR, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/11604**
	REV	**PAGE** 1 **OF** 14

AMSC N/A

5962-V014-11

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance variable resolution, 10-bit to 16-bit R/D converter with reference oscillator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/11604	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD2S1210-EP	Variable resolution, 10-bit to 16-bit R/D converter with reference Oscillator

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	JEDEC MS026	Low profile Quad Flat Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage referenced :
- AV_{DD} to AGND, DGND ..... -0.3 V to +7.0 V
- DV_{DD} to AGND, DGND ..... -0.3 V to +7.0 V
- V_{DRIVE} to AGND, DGND ..... -0.3 V to AV_{DD}
- AGND to DGND ..... -0.3 V to +0.3 V

Analog input voltage to AGND ..... -0.3 V to AV_{DD} + 0.3 V
Digital input voltage to DGND ..... -0.3 V to V_{DRIVE} + 0.3 V
Digital output voltage to DGND ..... -0.3 V to V_{DRIVE} + 0.3 V
Analog output voltage swing ..... -0.3 V to AV_{DD} + 0.3 V
Input current to any pin except supplies 2/ ..... ±10 mA
Ambient operating temperature range ..... -55°C to +125°C
Storage temperature range ..... -65°C to +150°C
Thermal resistance, junction to ambient (θ_{JA}) 3/ ..... 54°C /W
Thermal resistance, junction to case (θ_{JC}) 3/ ..... 15°C /W
RoHS Compliant temperature, soldering reflow ..... 260(-5/+0) °C
Electro Static Discharge (ESD) ..... 2 kV HBM

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC STD 51-2 – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Transient currents of up to 100 mA do not cause latch-up
3/ JEDEC 2S2P standard board (JEDEC 51-2 high-thermal-conductivity (high K**)** PCB**)**.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Test conditions 2/ unless otherwise specified	Limits		Unit
		Min	Max	
Sine, Cosine inputs 3/				
Voltage amplitude	Sinuosoidal waveforms, differential SIN to SINLO, COS to COSLO	2.3	4.0	Vp-p
Input bias current	V_{IN} = 4.0 Vp-p, CLKIN = 8.192 MHz		8.25	µA
Input impedance		485		kΩ
Phase lock range	Sine/Cosine vs EXC output, Control register D3 = 0	-44	+44	°
Common mode rejection		±20 TYP		arc sec/V
Angular accuracy 4/				
Angular accuracy			±7 + 1 LSB	arc min
Resolution	No missing code	10, 12, 14, 16 TYP		bits
Linearity INL				
10-bit			±1	LSB
12-bit			±2	
14-bit			±4	
16-bit			±16	
Linearity DNL			±0.9	LSB
Repeatability		±1		LSB
Velocity output				
Velocity accuracy 5/				
10-bit	Zero acceleration		±2	LSB
12-bit			±2	
14-bit			±4	
16-bit			±16	
Resolution 6/		9, 11, 13, 15 TYP		bits
Dynamic Performance				
Bandwidth				
10-bit		2000	6600	Hz
	CLKIN = 8.192 MHz	2900	5400	
12-bit		900	2800	
	CLKIN = 8.192 MHz	1200	2200	
14-bit		400	1500	
	CLKIN = 8.192 MHz	600	1200	
16-bit		100	350	
	CLKIN = 8.192 MHz	125	275	
Tracking rate				
10 bit	CLKIN = 10.24 MHz		3125	rps
	CLKIN = 8.192 MHz		2500	
12-bit	CLKIN = 10.24 MHz		1250	rps
	CLKIN = 8.192 MHz		1000	
14-bit	CLKIN = 10.24 MHz		625	rps
	CLKIN = 8.192 MHz		500	
16-bit	CLKIN = 10.24 MHz		156.25	rps
	CLKIN = 8.192 MHz		125	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
Dynamic performance – Continued.					
Acceleration Error					
10-bit		At 50,000 rps 3/, CLKIN = 8.129 MHz	30 TYP		arc min
12-bit		At 10,000 rps 3/, CLKIN = 8.129 MHz	30 TYP		
14-bit		At 2,500 rps 3/, CLKIN = 8.129 MHz	30 TYP		
16-bit		At 125 rps 3/, CLKIN = 8.129 MHz	30 TYP		
Setting time 10° step input					
10-bit		To settle to within ±2 LSB, CLKIN = 8.192 MHz		0.9	ms
12-bit		To settle to within ±2 LSB, CLKIN = 8.192 MHz		3.3	
14-bit		To settle to within ±2 LSB, CLKIN = 8.192 MHz		9.8	
16-bit		To settle to within ±2 LSB, CLKIN = 8.192 MHz		48	
Setting time 179° step input					
10-bit		To settle to within ±2 LSB, CLKIN = 8.192 MHz		2.4	ms
12-bit		To settle to within ±2 LSB, CLKIN = 8.192 MHz		6.1	
14-bit		To settle to within ±2 LSB, CLKIN = 8.192 MHz		15.2	
16-bit		To settle to within ±2 LSB, CLKIN = 8.192 MHz		68	
EXC, $\overline{\text{EXC}}$, Outputs					
Voltage		Load ±100 µA, typical differential output (EXC to $\overline{\text{EXC}}$) = 7.2 Vp-p	3.2	4.0	Vp-p
Center voltage			2.4	2.53	V
Frequency			2	20	kHz
EXC/$\overline{\text{EXC}}$ DC Mismatch				30	mV
EXC/$\overline{\text{EXC}}$ AC Mismatch				132	mV
THD			-58 TYP		dB
Voltage reference					
REFOUT		$\pm I_{OUF}$ = 100 µA	2.4	2.53	V
Drift			100 TYP		ppm/°C
PSRR			-60 TYP		dB
CLKIN, XTALOUT 7/					
Voltage input low	V_{IL}			0.8	V
Voltage input high	V_{IH}		2.0		
Logic inputs					
Voltage input low	V_{IL}	V_{DRIVER} = 2.7 V to 5.25 V V_{DRIVER} = 2.3 V to 2.7 V		0.8 0.7	V
Voltage input high	V_{IH}	V_{DRIVER} = 2.7 V to 5.25 V V_{DRIVER} = 2.3 V to 2.7 V	2.0 1.7		
Low level input current (Non Pull-Up)	I_{IL}			10	µA
Low level input current (Pull-Up)	I_{IL}	RES0, RES1, $\overline{\text{RD}}$, $\overline{\text{WR/FSYNC}}$, A0, A1, and $\overline{\text{RESET}}$ pins		80	
High level input current	I_{IH}		-10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
Logic outputs					
Voltage output low	V_{OL}	V_{DRIVER} = 2.3 V to 2.7 V		0.4	V
Voltage output high	V_{OH}	V_{DRIVER} = 2.7 V to 5.25 V V_{DRIVER} = 2.3 V to 2.7 V	2.4 2.0		
High level three-state leakage	I_{OZH}		-10		µA
Low level three-state leakage	I_{OZL}			10	
Power requirements					
AV_{DD}			4.75	5.25	V
DV_{DD}			4.75	5.25	
V_{DRIVE}			2.3	5.25	
Power supply					
I_{AVDD}				12	mA
I_{DVDD}				35	
I_{OVDD}				2	
Timing					
Frequency of clock input	f_{CLKIN}		6.144	10.24	MHz
Clock period (t_{CK} = 1/f_{CLKIN})	t_{CK}		98	163	ns
A0 and A1 setup time before $\overline{RD}/\overline{CS}$ low	t_1		2		
Delay $\overline{CS}$ falling edge to $\overline{WR}/\overline{FSYNC}$ rising edge	t_2		22		
Address/data setup time during a write cycle	t_3		3		
Address/data hold time during a write cycle	t_4		2		
Delay $\overline{WR}/\overline{FSYNC}$ rising edge to $\overline{CS}$ rising edge	t_5		2		
Delay $\overline{CS}$ rising edge to $\overline{CS}$ falling edge	t_6		10		
Delay between writing address and writing data	t_7		2 x t_{CK} + 20		
A0 and A1 hold time after $\overline{WR}/\overline{FSYNC}$ rising edge	t_8		2		
Delay between successive write cycles	t_9		6 x t_{CK} + 20		
Delay between rising edge of $\overline{WR}/\overline{FSYNC}$ and falling edge of $\overline{RD}$	t_{10}		2		
Delay $\overline{CS}$ falling edge to $\overline{RD}$ falling edge	t_{11}		2		
Enable delay $\overline{RD}$ low to data valid in configuration mode:	t_{12}	V_{DRIVE} = 4.5 V to 5.25 V V_{DRIVE} = 2.7 V to 3.6 V V_{DRIVE} = 2.3 V to 2.7 V	37 25 30		
$\overline{RD}$ rising edge to $\overline{CS}$ rising edge	t_{13}		2		
Disable delay $\overline{RD}$ high to data high-Z	t_{14A}		16		
Disable delay $\overline{CS}$ high to data high-Z	t_{14B}		16		
Delay between rising edge of $\overline{RD}$ and falling edge of $\overline{WR}/\overline{FSYNC}$	t_{15}		2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
Timing - Continued					
$\overline{\text{SAMPLE}}$ pulse width	t_{16}		2 x t_{CK} + 20		ns
Delay from $\overline{\text{SAMPLE}}$ before $\overline{\text{RD}}/\overline{\text{CS}}$ low	t_{17}		6 x t_{CK} + 20		
Hold time $\overline{\text{RD}}$ before $\overline{\text{RD}}$ low	t_{18}		2		
Enable delay $\overline{\text{RD}}/\overline{\text{CS}}$ low to data valid	t_{19}	V_{DRIVE} = 4.5 V to 5.25 V V_{DRIVE} = 2.7 V to 3.6 V V_{DRIVE} = 2.3 V to 2.7 V	17 21 33		
$\overline{\text{RD}}$ pulse width	t_{20}		6		
A0 and A1 set time to data valid when $\overline{\text{RD}}/\overline{\text{CS}}$ low	t_{21}	V_{DRIVE} = 4.5 V to 5.25 V V_{DRIVE} = 2.7 V to 3.6 V V_{DRIVE} = 2.3 V to 2.7 V	36 37 29		
Delay $\overline{\text{WR}}/\overline{\text{FSYNC}}$ falling edge to SCLK rising edge	t_{22}		3		
Delay $\overline{\text{WR}}/\overline{\text{FSYNC}}$ falling edge to SDO release from high-Z	t_{23}	V_{DRIVE} = 4.5 V to 5.25 V V_{DRIVE} = 2.7 V to 3.6 V V_{DRIVE} = 2.3 V to 2.7 V	16 26 29		
Delay SCLK rising edge to DBx valid	t_{24}	V_{DRIVE} = 4.5 V to 5.25 V V_{DRIVE} = 2.7 V to 3.6 V V_{DRIVE} = 2.3 V to 2.7 V	24 18 32		
SCLK high time	t_{25}		0.4 x t_{CK}		
SCLK low time	t_{26}		0.4 x t_{CK}		
SDI setup time prior to SCLK falling edge	t_{27}		3		
SDI hold time after SCLK falling edge	t_{28}		2		
Delay $\overline{\text{WR}}/\overline{\text{FSYNC}}$ rising edge to SDO high-Z	t_{29}		15		
Delay from $\overline{\text{SAMPLE}}$ before $\overline{\text{WR}}/\overline{\text{FSYNC}}$ falling edge	t_{30}		6 x t_{CK} + 20		
Delay $\overline{\text{CS}}$ falling edge to $\overline{\text{WR}}/\overline{\text{FSYNC}}$ falling edge in normal mode	t_{31}		2		
A0 and A1 setup time before $\overline{\text{WR}}/\overline{\text{FSYNC}}$ falling edge	t_{32}		2		
A0 and A1 setup time before $\overline{\text{WR}}/\overline{\text{FSYNC}}$ falling edge 8/	t_{33}	In normal mode, A0 = 0, A1 = 0/1 In configuration mode, A0 = 1, A1 = 1	24 x t_{CK} + 5 8 x t_{CK} + 5		
Delay $\overline{\text{WR}}/\overline{\text{FSYNC}}$ rising edge to $\overline{\text{WR}}/\overline{\text{FSYNC}}$ falling edge	t_{34}		10		
Frequency of SCLK input	f_{SCLK}	V_{DRIVE} = 4.5 V to 5.25 V V_{DRIVE} = 2.7 V to 3.6 V V_{DRIVE} = 2.3 V to 2.7 V	20 25 15		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ AV_{DD} = DV_{DD} = 5 V ±5%, CLKIN = 8.192 MHz ±25%, EXC, $\overline{EXC}$ frequency = 10 kHz to 20 kHz (10 bit); 6 kHz to 20 kHz (12 bit); 3 kHz to 12 kHz (14 bit); 2 kHz to 10 kHz (16 bit); T_A = -55°C to 125°C (unless otherwise noted).

3/ The voltages SIN, SINLO, COS and COSLO, relative to AGND, must always be between 0.15 V and AV_{DD} – 0.2 V.

4/ All specifications within the angular accuracy parameter are tested at constant velocity, that is, zero acceleration.

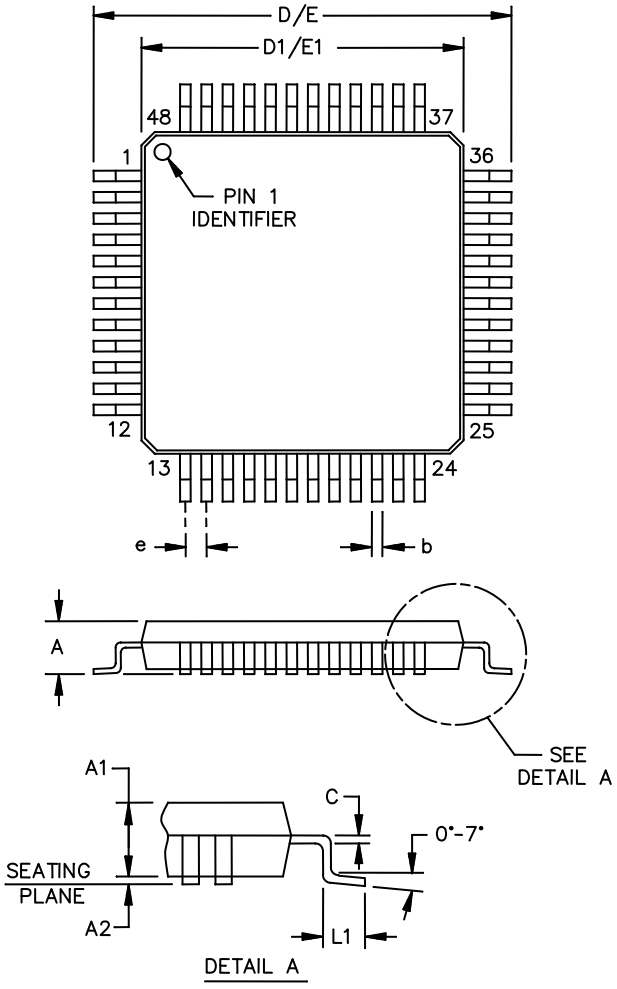
5/ The velocity accuracy specification includes velocity offset and dynamic ripple.

6/ For example, when RESO = 0 and RES1 = 1, the position output has a resolution of 12 bits. The velocity output has a resolution of 11 bits with the MSB indicating the direct of rotation. In this example, with a CLKIN frequency of 8.192 MHz, the velocity LSB is 0.488 rps, that is 1000 rps (2^{11}).

7/ The clock frequency of this device can be supplied with a crystal, an oscillator, or directly from a DSP/microprocessor digital output. When using a signle-ended clock signal directly from the DSP/microprocessor, the XTALOUT pin should remain open circuit and the logic levels outlined under the logic inputs parameters in Table I apply.

8/ A0 and A1 should remain constant for the duration of the serial readback. This may required 24 clock periods to read back the 8 bit fault information in addition to the 16 bits of positions/velocity data. If the fault information is not required, A0/A1 may be released after 16 clock cycles.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.60	D/E	8.80	9.20
A1	1.35	1.45	D1/E1	6.80	7.20
A2	0.05	0.15	e	0.50 BSC	
b	0.17	0.27	L1	0.45	0.75
C	0.09	0.20			

FIGURE 1. Case outline.

Case outline X

Pin No.	Mnemonic	Description
1	RES1	Resolution Select 1. Logic input. RES1 in conjunction with RES0 allows the resolution of the AD2S1210-EP to be programmed.
2	$\overline{\text{CS}}$	Chip Select. Active low logic input. The device is enabled when $\overline{\text{CS}}$ is held low.
3	$\overline{\text{RD}}$	Edge-Triggered Logic Input. When the $\overline{\text{SOE}}$ pin is high, this pin acts as a frame synchronization signal and output enable for the parallel data outputs, DB15 to DB0. The output buffer is enabled when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are held low. When the $\overline{\text{SOE}}$ pin is low, the $\overline{\text{RD}}$ pin should be held high.
4	$\overline{\text{WR/FSYNC}}$	Edge-Triggered Logic Input. When the $\overline{\text{SOE}}$ pin is high, this pin acts as a frame synchronization signal and input enable for the parallel data inputs, DB7 to DB0. The input buffer is enabled when $\overline{\text{CS}}$ and $\overline{\text{WR/FSYNC}}$ are held low. When the $\overline{\text{SOE}}$ pin is low, the $\overline{\text{WR/FSYNC}}$ pin acts as a frame synchronization signal and enable for the serial data bus.
5, 19	DGND	Digital Ground. These pins are ground reference points for digital circuitry on the AD2S1210-EP. Refer all digital input signals to this DGND voltage. Both of these pins can be connected to the AGND p[lane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
6	DV_{DD}	Digital Supply voltage, 4.75 V to 5.25 V. This is the supply voltage for all digital circuitry on the AD2S1210-EP. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
7	CLKIN	Clock Input. A crystal or oscillator can be used at the CLKIN and XTALOUT pins to supply the required clock frequency of the AD2S1210-P. Alternatively, a single-ended clock can be applied to the CLKIN pin. The input frequency of the AD2S1210-EP is specified from 6.144 MHz to 10.24 MHz.
8	XTALOUT	Crystal Output. When using a crystal or oscillator to supply the clock frequency to the AD2S1210-EP, apply the crystal across the CLKIN and XTALOUT pins. When using a single-ended clock source, the XTALOUT pin should be considered a no connect pin.
9	$\overline{\text{SOE}}$	Serial Output Enable. Logic input. This pin enables either the parallel or serial interface. The serial interface is selected by holding the $\overline{\text{SOE}}$ pin low, and the parallel interface is selected by holding the $\overline{\text{SOE}}$ pin high.
10	$\overline{\text{SAMPLE}}$	Sample Result. Logic input. Data is transferred from the position and velocity integrators to the position and velocity registers after a high-to-low transition on the $\overline{\text{SAMPLE}}$ signal. The fault register is also updated after a high-to-low transition on the $\overline{\text{SAMPLE}}$ signal.
11	DB15/SDO	Data Bit 15/Serial Data Output Bus. When the $\overline{\text{SOE}}$ pin is high, this pin acts as DB15, a three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. When the $\overline{\text{SOE}}$ pin is low, this pin acts as SDO, the serial data output bus controlled by $\overline{\text{CS}}$ and $\overline{\text{WR/FSYNC}}$. The bits are clocked out on the rising edge of SCLK.
12	DB14/SDI	Data Bit 14/Serial Data Input Bus. When the $\overline{\text{SOE}}$ pin is high, this pin acts as DB14, a three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. When the $\overline{\text{SOE}}$ pin is low, this pin acts as SDI, the serial data input bus controlled by $\overline{\text{CS}}$ and $\overline{\text{WR/FSYNC}}$. The bits are clocked in on the falling edge of SCLK.
13	DB13/SCLK	Data Bit 13/Serial Clock. In parallel mode, this pin acts as DB13, a three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. In serial mode, this pin acts as the serial clock input.
14 to 17	DB12 to DB9	Data Bit 12 to Data Bit 9. Three-state data output pins controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$.
18	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage range on this pin is 2.3 V to 5.25 V and may be different from the voltage range at AV_{DD} and DV_{DD} but should never exceed either by more than 0.3 V.
20	DB8	Data Bit 8. Three-state output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$.
21 to 28	DB7 to DB0	Data Bit 7 to Data Bit 0. Three-state data input/output pins controlled by $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR/FSYNC}}$.

FIGURE 2. Terminal connections.

Case outline X

Pin No.	Mnemonic	Description
29	A	Incremental Encoder Emulation Output A. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.
30	B	Incremental Encoder Emulation Output B. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.
31	NM	North Marker Incremental Encoder Emulation Output. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.
32	DIR	Direction. Logic output. This output is used in conjunction with the incremental encoder emulation outputs. The DIR output indicates the direction of the input rotation and is high for increasing angular rotation.
33	$\overline{\text{RESET}}$	Reset. Logic input. The AD2S1210-EP requires an external reset signal to hold the $\overline{\text{RESET}}$ input low until V_{DD} is within the specified operating range of 4.75 V to 5.25 V.
34	LOT	Loss of Tracking. Logic output. Loss of tracking (LOT) is indicated by a logic low on the LOT pin and is not latched.
35	DOS	Degradation of Signal. Logic output. Degradation of signal (DOS) is detected when either resolver input (sine or cosine) exceeds the specified DOS sine/cosine threshold or when an amplitude mismatch occurs between the sine and cosine input voltages. DOS is indicated by a logic low on the DOS pin.
36	A1	Mode Select 1. Logic input. A1 in conjunction with A0 allows the mode of the AD2S1210-EP to be selected.
37	A0	Mode Select 0. Logic input. A0 in conjunction with A1 allows the mode of the AD2S1210-EP to be selected.
38	EXC	Excitation Frequency. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ($\overline{\text{EXC}}$) to the resolver. The frequency of this reference signal is programmable via the excitation frequency register.
39	$\overline{\text{EXC}}$	Excitation Frequency Complement. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ($\overline{\text{EXC}}$) to the resolver. The frequency of this reference signal is programmable via the excitation frequency register.
40	AGND	Analog Ground. This pin is the ground reference points for analog circuitry on the AD2S1210-EP. Refer all analog input signals and any external reference signal to this AGND voltage. Connect the AGND pin to the AGND plane of a system. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
41	SIN	Positive Analog Input of Differential SIN/SINLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
42	SINLO	Negative Analog Input of Differential SIN/SINLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
43	AV_{DD}	Analog Supply Voltage, 4.75 V to 5.25 V. This pin is the supply voltage for all analog circuitry on the AD2S1210-EP. The AV_{DD} and DV_{DD} voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
44	COSLO	Negative Analog Input of Differential COS/COSLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
45	COS	Positive Analog Input of Differential COS/COSLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
46	REFBYP	Reference Bypass. Connect reference decoupling capacitors at this pin. Typical recommended values are 10 µF and 0.01 µF.
47	REFOUT	Voltage Reference Output.
48	RES0	Resolution Select 0. Logic input. RES0 in conjunction with RES1 allows the resolution of the AD2S1210-EP to be programmed.

FIGURE 2. Terminal connections - Continued.

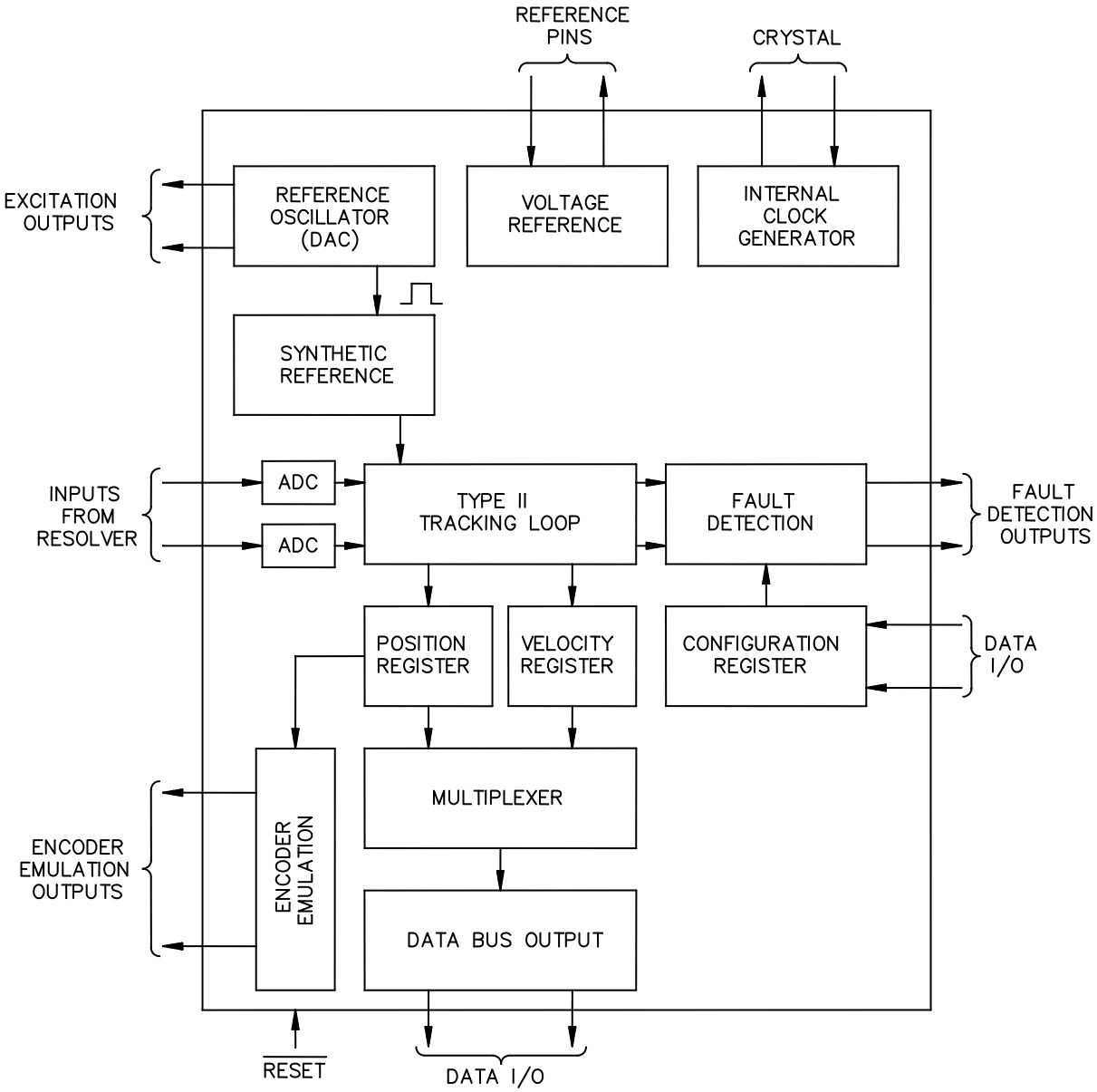


FIGURE 3. Functional block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/11604-01XB	24355	AD2S1210SST-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605